

## Optimizing ATE resources for ATPG patterns

### Background

ATPG patterns today often feature clock signals declared as extensions to default timing in STIL files. Hence, these clock signals use traditional ATE formats NRZ and RZ/R1. It would be desirable to optimize the clock format usage to RZ/R1 if feasible. An enhancement to the WDBconditioner enables clock signal timing optimization for ATE.

To illustrate the situation, consider the following example. The timing section of an example STIL file is shown in Figure 1. It can be seen that the signal called *TCK* (an input signal) has timing declared by the group *all\_inputs* and the *TCK* row. Hence *TCK* has STIL WaveformCharacters 01ZN (NRZ) and P (pulse-high). Given this information, it is not possible to optimize the timing to traditional RZ (off-low and pulse-high) given that another steady state level (1) is declared. Hence to correctly optimize requires an analysis of pattern to ensure that the 1 WaveformCharacter is not being used.

```
Timing {
  WaveformTable "_allclock_launch_capture_WFT_" {
    Period '100ns';
    Waveforms {
      "all_inputs" { 0 { '0ns' D; } }
      "all_inputs" { 1 { '0ns' U; } }
      "all_inputs" { Z { '0ns' Z; } }
      "all_inputs" { N { '0ns' N; } }
      "all_outputs" { X { '0ns' X; '39ns' X; } }
      "all_outputs" { H { '0ns' X; '39ns' H; } }
      "all_outputs" { L { '0ns' X; '39ns' L; } }
      "all_outputs" { T { '0ns' X; '39ns' T; } }
      "TCK" { P { '0ns' D; '40ns' U; '70ns' D; } }
    }
  }
}
```

Figure 1: Timing section from a typical ATPG-generated STIL file.

### Example Setup

Consider the following basic scenario shown below in Figure 2.

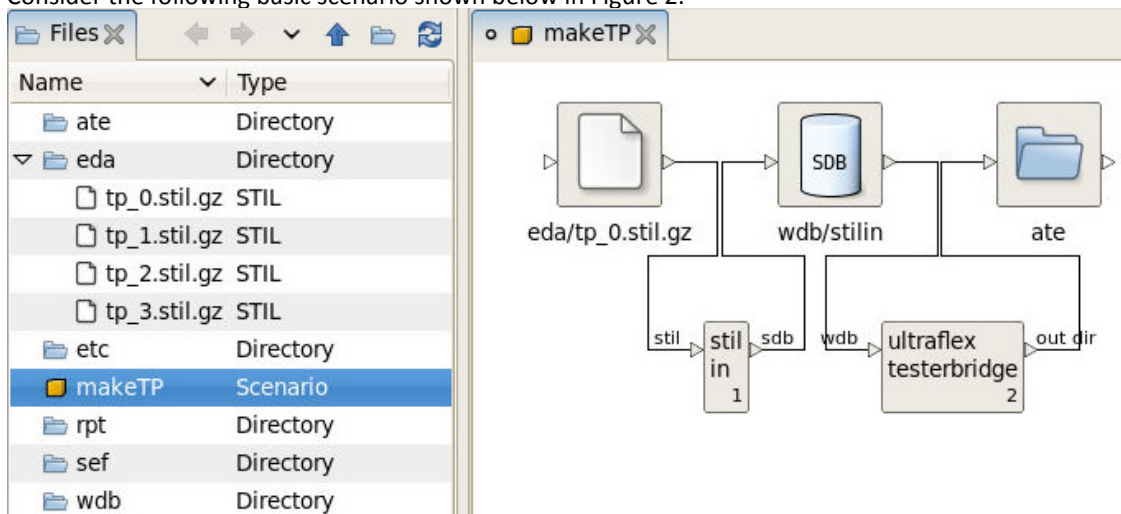
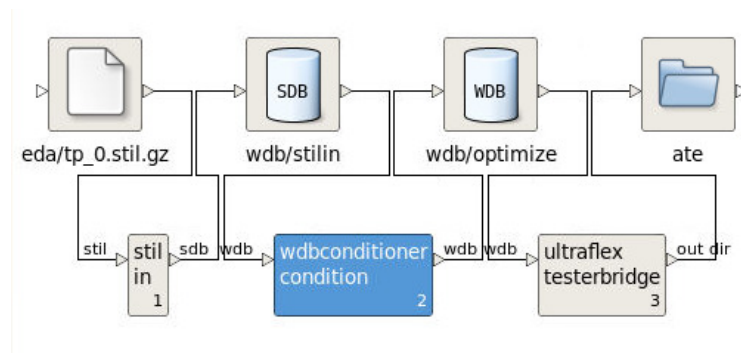


Figure 2: Typical ATPG translation scenario.

In order to optimize the clock signals, we will need to add an WDBconditioner stage. You can choose to optimize in-situ (replace WDB) or generate a new WDB. The scenario below in Figure 3 shows the later case (generate new WDB)



**Figure 3: Example Scenario with WDBconditioner stage**

The parameters can be chosen for desired operation:

WDBCONDITIONER Conditioner. Operation 2.

use operation file?	<input type="text" value="NO"/>
operation:	<input type="text" value="TIMEPLATE_OPTIMIZE"/>
source WDB 1:	<input type="text" value="wdb/stilin"/>
use dest WDB?	<input type="text" value="YES"/>
destination WDB:	<input type="text" value="wdb/optimize"/>
remove unused tps?	<input type="text" value="NO"/>
remove duplicate tps?	<input type="text" value="NO"/>
remove unused tracks?	<input type="text" value="YES"/>
optimize clock shapes?	<input type="text" value="YES"/>

**Figure 4: Parameters for WDBconditioner stage**

- remove unused tps?      Selects whether the timeplate optimize operation will delete unused timeplates (tps).
- remove duplicate tps?      Selects whether the timeplate optimize operation will delete duplicate timeplates.
- remove unused tracks?      Selects whether the timeplate optimize operation will delete unused timeplate tracks.
- optimize clock shapes?      Selects whether to convert non-sampled clock shapes into ATE format shapes.

Consider the above example shown in Figure 1. Using the Timing Editor to view the TimePlate derived from ATPG STIL Timing declaration for *allclock\_launch\_capture\_WFT* is shown in Figure 5 is below. It can be seen that there two force timing tracks/rows for TCK – one a S and one a DUD shape. After running the scenario, using the Timing Editor to examine the optimized in Figure 6 below, it can be seen that the TCK signal now has only one timing tracks/rows – PSD (which maps to a “RZ” shape on most ATE systems, using only Timing Generator strobes). The WDBconditioner performed an analysis of the source WDB and determined that the “1/Z” tracks were not in use.

Further optimization can be obtained by *selecting remove unused tracks?* to YES.

Creating a set of timing and pattern files for the Ultraflex, it can be seen in the IG-XL Timing File that the format RL has been selected for the signal TCK. With the original DUD/NRZ shape, the SBL format would have been chosen to ensure that there was a transition at T1 time. See Figure 7.

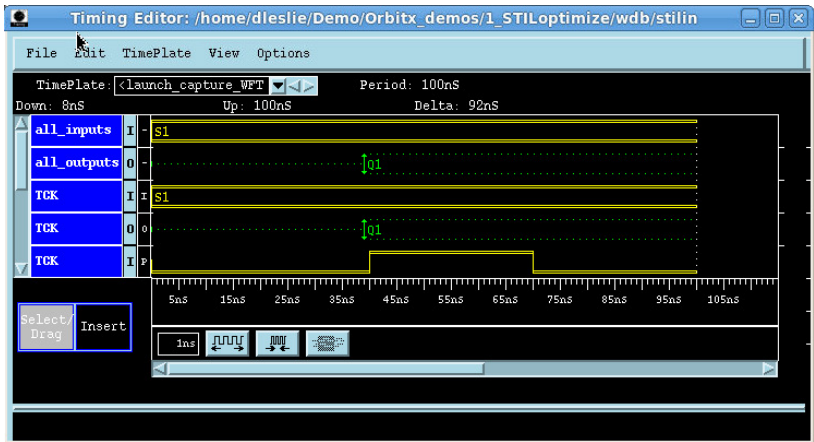


Figure 5: Timing Editor showing STIL file

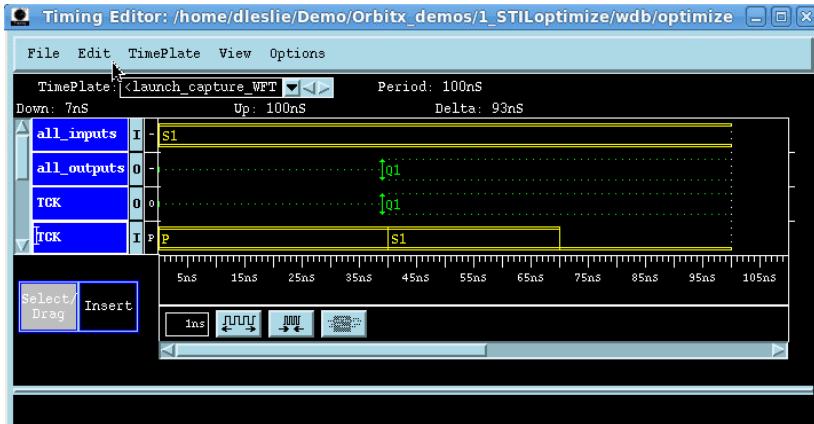


Figure 6: Timing Editor showing TimePlate with optimized shape choice for TCK

Time Set	Period	Name	Setup	Src	Fmt	On	Data	Return
allclock_launch_capture_WFT	=100*ns	all_inputs	i/o	PAT	NR	0	0	0
allclock_launch_capture_WFT	=100*ns	all_outputs	i/o	PAT	NR	0	0	0
allclock_launch_capture_WFT	=100*ns	TCK	i/o	PAT	RL	0	=40*ns	=70*ns

Figure 7: Partial Ultraflex Timing File with the RL format highlighted on signal TCK (edited for clarity)