TSSI TD-ScanPRO Optimizes Timing Across Multiple ATPG Files

1. Introduction

DFT teams often deliver many ATPG files in the standard file format such as WGL or STIL for testing the same device. Each ATPG file has its own timing and pattern. Some timings are common across all the ATPG files. Some are not. For instance, the timing for scan shift cycles is different from launch and capture cycles.

Most conversion tools generate a corresponding NI STS timing file (.digitiming) and NI STS pattern file (.digipat) per input ATPG file, which is fine for testing one timing/pattern pair at a time. However, executing all patterns is best to have a single master timing for all test patterns.

The benefit is the optimal usage of the precious time-set resources on the tester, and also the saving of re-loading different time-sets for each pattern execution.

2. Using TD-ScanPRO's "Orbitx" and "Incremental" Conditioners

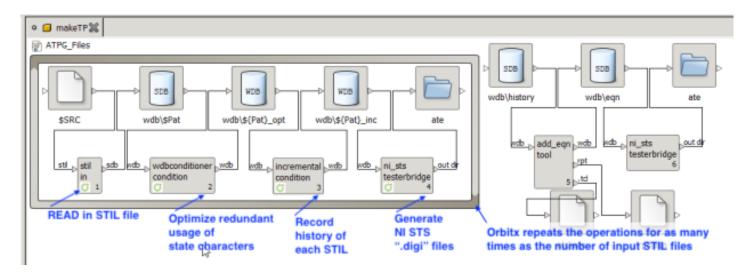


Figure 1: A Sample Setup of TD-ScanPRO Scenario Using Orbitx and Incremental Conditioners

Shown in Figure 1 are operations to convert 4 ATPG STIL files:

- 1. The "STIL In" operation to read in an ATPG file in the STIL format
- 2. The "wdbconditioner" operation is optional, but highly recommended, to pre-condition the STIL file for the optimal usage of state characters, which varies from one ATPG tool to another. TSSI TD-ScanPRO covers all variations.
- 3. The "Incremental" conditioner is the key step to record timing history found in each and every incoming STIL file to "learn" the timing behavior across all files
- 4. The "NI_STS" Testerbridge generates an NI STS pattern for each incoming STIL file
- 5. The "Orbitx" object that encompasses the 4 operations repeats them as many times as the number of incoming STIL files fed into the flow
- 6. The Add Equation ("add_eqn") operation is optional but useful in adding variables to timing for spec-based operations on the tester such as Shmoo.
- 7. The last "NI_STS" Testerbridge step, outside of the Orbitx loop, takes the History database ("wdb/history") as an input to generate a single master timing that serves all of the incoming ATPG patterns

3. The Resultant Files

Figure 2 shows the NI STS files generated by the described TD-ScanPRO's flow above after processing 4 input STIL files.

| 🔀 myChip.pinmap | |
|-------------------|--|
| | |
| 📰 myChip.specs | |
| myChip.digitiming | |
| myChip.digilevels | |
| 만 tp_0.digipat | |
| 한번 tp_1.digipat | |
| 한 tp_2.digipat | |
| 肥 tp_3.digipat | |

Figure 2: The resultant files from processing 4 input STIL files

There are 4 NI STS patterns loaded into the NI Pattern Editor: tp_0.digipat, tp_1.digipat, tp_2.digipat, and tp_3.digipat. There is only one NI STS timing file, myChip.digitiming (as shown in Figure 3), that serves all 4 pattern files.

| r N | lame | Period | Pin Item | Edge Multiplier | Drive Format | Drive On | Drive Data | Drive Return | Drive Off | Compare Strobe | C | |
|-----|-----------|--------------------|---------------|-----------------|--------------|----------|--------------------|--------------------|--------------------|--------------------|---|--|
| P | ar_NFT | ControlSet1.tper_0 | 61_all_inputs | 1x | NR | θs | 0 s | | 40 ns | 0 s | | |
| р | ar_WFT | ControlSet1.tper_0 | all_outputs | 1x | NR | 0 s | 0 s | | ControlSet1.tper_0 | ControlSet1.po01_1 | | |
| р | ar_WFT | ControlSet1.tper_0 | pclk | 1x | RL | 0 5 | ControlSet1.pclk_1 | ControlSet1.pclk_2 | 40 ns | 0 s | | |
| р | ar_WFT | ControlSet1.tper_0 | sclk | 1x | RH | 0 s | ControlSet1.sclk_1 | ControlSet1.sclk_2 | 40 ns | 0 s | | |
| р | ar_WFT_1 | controlSet1.tper_0 | 61_all_inputs | 1x | NR | 0 s | 0 s | | 40 ns | 0 s | | |
| р | ar_WFT_1 | ControlSet1.tper_0 | all_outputs | 1x | NR | 0 s | 0 s | | ControlSet1.tper_0 | ControlSet1.po01_1 | | |
| р | ar_WFT_1 | controlSet1.tper_0 | pclk | 1x | RL | 0 5 | ControlSet1.pclk_1 | ControlSet1.pclk_3 | 40 ns | 0 s | | |
| р | ar_WFT_1 | ControlSet1.tper_0 | sclk | 1x | RH | 0 s | ControlSet1.sclk_1 | ControlSet1.sclk_3 | 40 ns | 0 s | | |
| р | ar_WFT_2 | ControlSet1.tper_0 | G1_all_inputs | 1x | NR | 0 s | 0 s | | 40 ns | 0 s | | |
| р | ar_WFT_2 | ControlSet1.tper_0 | all_outputs | 1x | NR | 0 s | 0 s | | ControlSet1.tper_0 | ControlSet1.po01_1 | | |
| р | ar_WFT_2 | controlSet1.tper_0 | pclk | 1x | RL | 0 s | ControlSet1.pclk_1 | ControlSet1.pclk_4 | 40 ns | 0 s | | |
| р | ar_WFT_2 | ControlSet1.tper_0 | sclk | 1x | RH | 0 s | ControlSet1.sclk_1 | ControlSet1.sclk_4 | 40 ns | 0 s | | |
| s | can_WFT | ControlSet1.tper_0 | G1_all_inputs | 1x | NR | 0 s | 0 s | | 40 ns | 0 s | | |
| s | can_WFT | ControlSet1.tper_0 | all_outputs | 1x | NR | 0 s | 0 s | | ControlSet1.tper_0 | ControlSet1.po01_1 | | |
| 5 | can_WFT | controlSet1.tper_0 | pclk | 1x | RL | 0 5 | ControlSet1.pclk_1 | ControlSet1.pclk_2 | 40 ns | 0 5 | | |
| s | can_WFT | ControlSet1.tper_0 | sclk | 1x | RH | 0 s | ControlSet1.sclk_1 | ControlSet1.sclk_2 | 40 ns | 0 s | | |
| s | can_WFT_1 | controlSet1.tper_0 | G1_all_inputs | 1x | NR | 0 s | 0 s | | 40 ns | 0 s | | |
| s | can_WFT_1 | ControlSet1.tper_0 | all_outputs | 1x | NR | 0 s | 0 s | | ControlSet1.tper_0 | ControlSet1.po01_1 | | |
| s | can_WFT_1 | ControlSet1.tper_0 | pclk | 1x | RL | 0 s | ControlSet1.pclk_1 | ControlSet1.pclk_2 | 40 ns | 0 s | | |
| 5 | can_WFT_1 | ControlSet1.tper_0 | sclk | 1x | RH | 0 s | ControlSet1.sclk_1 | ControlSet1.sclk_2 | 40 ns | 0 s | | |
| s | can_WFT_2 | ControlSet1.tper_0 | G1_all_inputs | 1x | NR | 0 s | 0 s | | 40 ns | 0 s | | |
| 5 | can_WFT_2 | ControlSet1.tper_0 | all_outputs | 1x | NR | 0 5 | 0 s | | ControlSet1.tper_0 | ControlSet1.po01_1 | | |
| s | can_WFT_2 | ControlSet1.tper_0 | pclk | 1x | RL | 0 s | ControlSet1.pclk_1 | ControlSet1.pclk_3 | 40 ns | 0 s | | |
| 5 | can_WFT_2 | controlSet1.tper_0 | sclk | 1x | RH | 0 s | ControlSet1.sclk_1 | ControlSet1.sclk_3 | 40 ns | 0 s | | |
| 5 | can_WFT_3 | ControlSet1.tper_0 | G1_all_inputs | 1x | NR | 0 s | 0 s | | 40 ns | 0 s | Γ | |
| 5 | can_WFT_3 | controlSet1.tper_0 | all_outputs | 1x | NR | 0 5 | 0 s | | ControlSet1.tper_0 | ControlSet1.po01_1 | Γ | |
| 5 | can_WFT_3 | controlSet1.tper_0 | pclk | 1x | RL | 0 s | ControlSet1.pclk_1 | ControlSet1.pclk_4 | 40 ns | 0 s | Γ | |
| 5 | can WFT 3 | ControlSet1.tper 0 | sclk | 1x | RH | 0 s | ControlSet1.sclk 1 | ControlSet1.sclk 4 | 40 ns | 0 s | Г | |

Figure 3: The single master NI STS time-set serves all 4 patterns

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